Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A semiconductor device comprising:
a substrate;
a device over the substrate;
a layer over the substrate and the device, the layer including at least one high aspect ratio opening and at least one low aspect ratio opening;
a rim within at least one high aspect ratio opening, the rim being at the depth of the at least one low aspect ratio opening, a diameter of the at least one high aspect ratio opening being smaller below the rim than above the rim; and
a coating material over the openings into the layer.

[c2] The semiconductor device of claim 1, wherein the layer is selected from a group consisting of silicon oxide, silicon dioxide, and hydrogenated silicon oxycarbide.

[c3] The semiconductor device of claim 1, wherein the at least one high aspect ratio opening has a sub-lithographic diameter below the rim.

[c4] A method of manufacturing a semiconductor device with openings of differing depths in a layer, the method com-

prising the steps of:

depositing a second layer onto a first layer having a plurality of devices;

forming a plurality of openings into the second layer, the plurality of openings including at least one high aspect ratio opening and at least one low aspect ratio opening;

depositing an etch-resistant mask layer onto the second layer such that the etch-resistant mask layer substantially coats the at least one low aspect ratio opening and at most partially coats the at least one high aspect ratio opening;

etching only the at least one high aspect ratio opening; and

depositing a coating material into the plurality of openings.

[c5] The method of claim 4, wherein the second layer is selected from a group consisting of silicon oxide, silicon dioxide, and hydrogenated silicon oxycarbide.

[c6] The method of claim 4, wherein the etch-resistant mask layer is selected from a group consisting of Si, SiO_2, Si_3N_4, W, and Cr.

[c7] The method of claim 4, wherein, before deposition of the etch resistant mask layer a) the at least one high aspect ratio opening has a diameter less than about one-half

the depth of the at least one high aspect ratio opening, and b) the at least one low aspect ratio opening has a diameter greater than about one-half the depth of the at least one low aspect ratio opening.

[c8] The method of claim 4, wherein the etch-resistant mask layer is deposited by an anisotropic technique selected from a group comprising physical vapor deposition (PVD), sputter deposition, and chemical vapor deposition (CVD).

[c9] The method of claim 4, wherein the at least one high aspect ratio opening is etched using Reactive Ion Etching (RIE).

[c10] The method of claim 4, further comprising the step of using an anisotripic etch, prior to etching the at least one high aspect ratio opening, to remove any etch-resistant mask layer from the bottom of the at least one high aspect ratio opening without removing the etch-resistant mask layer from the at least one low aspect ratio opening.

[c11] A method of protecting underlying structures during the manufacture of a semiconductor device, the method comprising the steps of:
depositing an interlevel layer onto an encapsulating layer

having a plurality of structures and residing atop a substrate, where the interlevel layer includes a material different from the material of the encapsulating layer;
forming at least one high aspect ratio opening by removing the interlevel layer from between the plurality of structures without removing the encapsulating layer;
depositing an etch-resistant mask layer onto the interlevel layer and exposed portions of the encapsulating layer such that the etch-resistant mask layer at most partially coats the at least one high aspect ratio opening and substantially coats the remaining surfaces of the interlevel layer and the encapsulating layer;
etching the encapsulating layer such that the at least one high aspect ratio opening is etched through to the substrate; and
depositing a coating material into the at least one high aspect ratio opening such that a connection is made to the substrate.

[c12] The method of claim 11, wherein the interlevel layer is selected from a group consisting of silicon oxide, silicon dioxide, and hydrogenated silicon oxycarbide.

[c13] The method of claim 11, wherein the encapsulating layer is selected from a group consisting of silicon nitride, silicon carbide, and siliconoxynitride.

[c14] The method of claim 11, wherein the etch-resistant mask layer is selected from a group consisting of Si, SiO_2, Si_3N_4, W, and Cr.

[c15] The method of claim 11, wherein the at least one high aspect ratio opening, before deposition of the etch-resistant mask layer, has a diameter less than about one-half the depth of the at least one high aspect ratio opening.

[c16] The method of claim 11, wherein the etch-resistant mask layer is deposited by an anisotropic technique selected from a group comprising physical vapor deposition (PVD) and sputter deposition.

[c17] The method of claim 11, wherein one or more of the interlevel layer and the encapsulating layer are etched using Reactive Ion Etching (RIE).

[c18] The method of claim 11, further comprising the step of removing any etch-resistant mask layer from the bottom of the at least one high aspect ratio opening without removing the etch-resistant mask layer from the remaining surfaces of the interlevel layer and the encapsulating layer prior to etching the at least one high aspect ratio opening.

[c19] The method of claim 18, wherein the removal of any

etch-resistant mask layer is by means of Reactive Ion Etching (RIE).

[c20] The method of claim 11, wherein the etching of the encapsulating layer through to the substrate has a diameter less than the diameter of the at least one high aspect ratio opening between the plurality of structures.